HANDS-ON — Memory Hierarchies in CPU/GPU Architectures

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https://tinyurl.com/cudafordummies/i/ho2/notes-ho2.pdf



CUDA 4 Dummies — Oct 24-25, 2023

HANDS-ON — Memory Hierarchies in CPU/GPU Architectures CUDA managed unified memory

Exercise

Q1) For a dummy kernel that does nothing else than reading the content of two arrays, a[] and b[], then adding together element by element and storing the results into a third array, c[], determine the bandwidth with the help of 'nsys nvprof' if we make use of cudaMallocManaged() and consider arrays of size 1 GB all throughout.



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CUDA MANAGED UNIFIED MEMORY CONT.

- A1) i) Examine the below sample program and adjust the dimension of the arrays in case, vi ./unified_memory_example_2.cu
 - ii) Compile and run it via the profiling toolchain nvcc unified_memory_example_2.cu nsys nvprof ./a.out and read out the time spent in KrnlDmmyCalc() ≈ 72394552 ns = 0.072394552 s



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Exercise

Q2) Considering the previous results, can we get closer to the theoretical memory bandwidth of 1555 GB/s if we call the compute kernel repeatedly within a loop over 100 iterations ? How would page faults change then and what else could we do to maximize bandwidth ?



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- A2) i) Yes, we can do better ! Get the below sample program, edit it and make sure that we really loop over 100 iterations, vi ./unified_memory_example_3.cu
 - *ii)* Again, compile it, run it, profile it and compute the obtained bandwidth from the profile(approximately 970 GB/s);
 - *iii)* The number of page faults will most likely have reduced now. Memory prefetching or usage of managed global device memory could further increase the bandwidth;

→ https://tinyurl.com/cudafordummies/i/l2/unified_memory_example_3.cu